SONY

CXD2552Q

1 Bit D/A Converter

Description

The CXD2552Q is 1 bit type D/A converter developed for digital audio products; compact disc player and others.

44 pin QFP (Plastic)

Features

- PLM pulse converter
- 3rd order noise shaper
- Direct digital sync
- Master clock 1024Fs
- 2 channel built in

Absolute Maximum Ratings

- Supply voltage V_{DD} −0.5 to +6.5 V
- Input voltage V_I −0.3 to V_{DD}+0.3 V
- Allowable power dissipation
  P_D 500 mW (Ta=60°C)
- Storage temperature
  Tstg −55 to +150 °C

Structure

Silicon gate CMOS IC

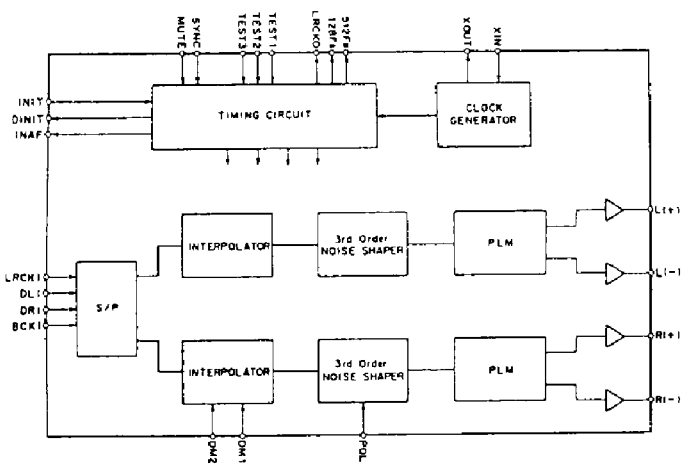
Applications

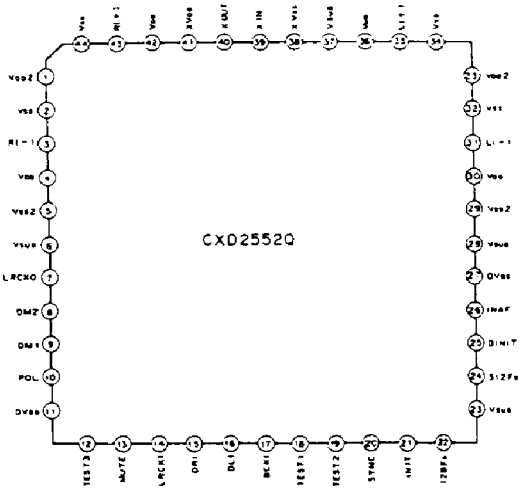
Compact disc player, digital amplifier, BS tuner

Recommended Operating Conditions

- Supply voltage V_{DD} 4.75 to 5.25 V
- Operating temperature Topr −10 to 60 °C
- OSC frequency fx 32.0 to 49.7 MHz
- Supply voltage difference
  V_{DD}–V_{DD2}, V_{DD}–DV_{DD}, V_{DD}–XV_{DD} ± 0.1V
  V_{SS}–V_{SS2}, V_{SS}–DV_{SS}, V_{SS}–XV_{SS} ± 0.1V

Block Diagram and Pin Configuration





Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD2}	—	Analog power supply
2	Vss	—	Analog GND
3	R (–)	O	Rch PLM output (Opposite phase)
4	V_{DD}	—	Analog power supply
5	V_{SS2}	—	Analog GND
6	V_{SUB}	—	Sub straight. Connect to GND.
7	LRCKO	O	LRCK output
8	DM2	I	Dither polarity
9	DM1	I	Dither designation
10	POL	I	PLM output polarity "L" : Positive phase "H" : Opposite phase
11	DV_{DD}	—	Digital power supply
12	TEST3	I	Test pin. Fixed at "L" level in normal operation mode.
13	MUTE	I	Turns interpolator output into 0 data. Effective at "H".
14	LRCKI	I	LRCK input
15	DRI	I	Rch data input
16	DLI	I	Lch data input
17	BCKI	I	BCK input
18	TEST1	I	Test pin. Fixed at "L" level in normal operation mode.
19	TEST2	I	Test pin.Fixed at "L" level in normal operation mode.
20	SYNC	I	Sync control pin
21	INIT	I	Resynchronized by rising edge of this signal
22	128Fs	O	128Fs output
23	V_{SUB}	—	Sub straight. Connect to GND.
24	512Fs	O	512Fs output
25	DINIT	O	Delay INIT signal output
26	INAF	O	When I/O sync is missed "H" is output.
27	DVss	—	Digital GND
28	V_{SUB}	—	Sub straight. Connect to GND.
29	V_{SS2}	—	Analog GND
30	V_{DD}	—	Analog power supply
31	L (–)	O	Lch PLM output (Opposite phase)
32	Vss	—	Analog GND
33	V_{DD2}	—	Analog power supply
34	Vss	—	Analog GND
35	L (+)	O	Lch PLM output (Positive phase)
36	V_{DD}	—	Analog power supply
37	V_{SUB}	—	Sub straight. Connect to GND.

Pin No.	Symbol	I/O	Description
38	XVss	——	Clock GND
39	XIN	I	Crystal oscillation input pin (1024Fs)
40	XOUT	O	Crystal oscillation output pin
41	XV_{DD}	——	Clock power supply
42	V_{DD}	——	Analog power supply
43	R (+)	O	Rch PLM output (Positive phase)
44	Vss	——	Analog GND

Electrical Characteristics

DC Characteristics

($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V \pm 5\%$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Topr=−10 to 60°C)

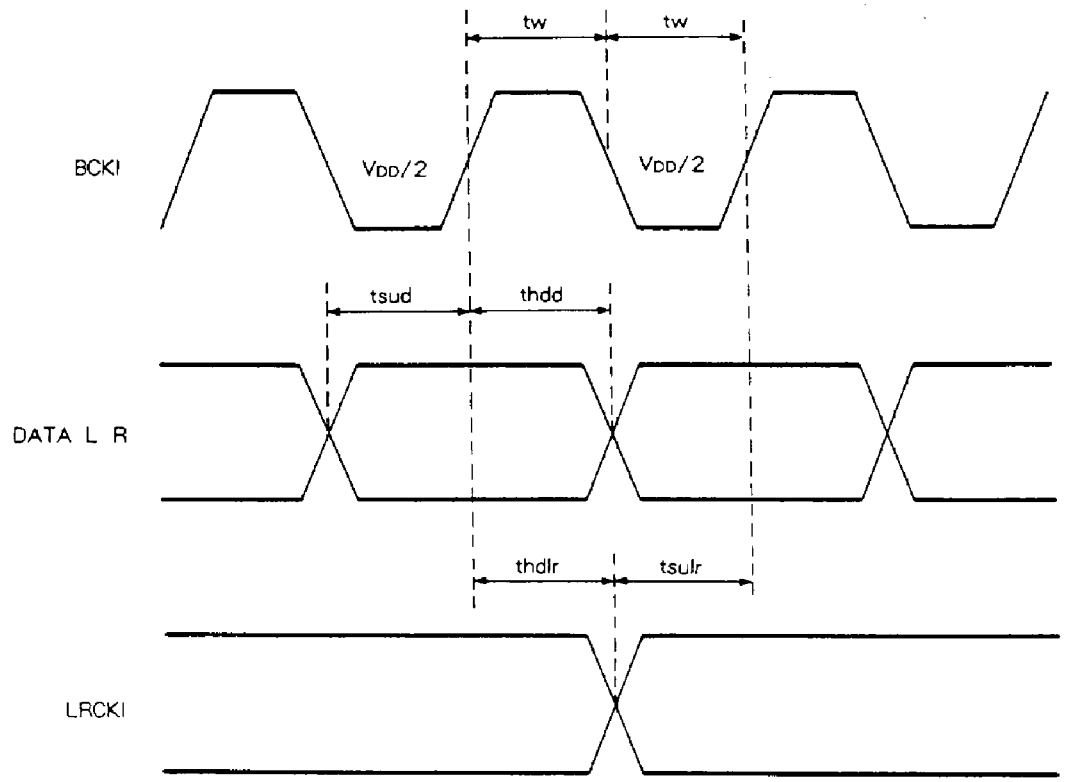
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	——	0.76V_{DD}			V
"L" input voltage	V_{IL}	——			0.24V_{DD}	V
Input leak current	I_{LI}	——			± 5.0	µA
"H" output voltage (DINIT, INAF)	V_{OH}	Io=−1mA	V_{DD}−0.5			V
"L" output voltage (DINIT, INAF)	V_{OL}	Io=1mA			0.4	V
"H" output voltage (512Fs, LRCKO)	V_{OH}	Io=−0.4mA	V_{DD}−0.5			V
"L" output voltage(512Fs, LRCKO)	V_{OL}	Io=0.4mA			0.4	V
"H" output voltage (128Fs)	V_{OH}	Io=−0.3mA	V_{DD}−0.5			V
"L" output voltage (128Fs)	V_{OL}	Io=0.3mA			0.4	V
"H" output voltage (R+, R−, L+, L−)	V_{OH}	Io=−15mA	V_{DD}−0.5			V
"L" output voltage (R+, R−, L+, L−)	V_{OL}	Io=15mA			0.5	V
"H" output voltage (XOUT)	V_{OH}	Io=−2.0mA	V_{DD}−0.5			V
"L" output voltage (XOUT)	V_{OL}	Io=2.0mA			0.4	V
Current consumption	I_{DD}	——		55	80	mA

AC Characteristics

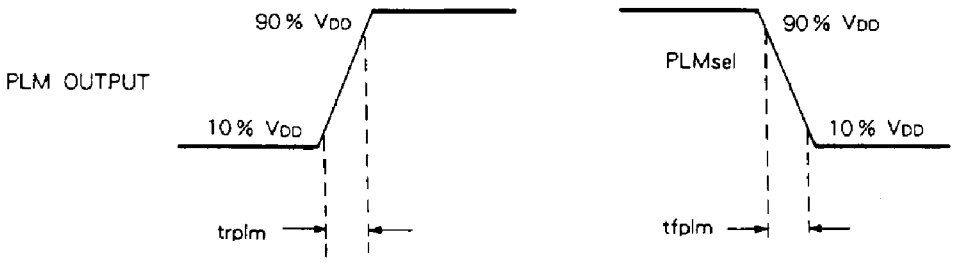
($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V \pm 5\%$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Topr=−10 to 60°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	tw		38			nsec
DATAL, R set up time	tsud		18			nsec
DATAL, R hold time	thdd		18			nsec
LRCKI set up time	tsulr		18			nsec
LRCKI hold time	thdlr		18			nsec
PLM output rise/fall time	tr, tf	CL=300pF		10		nsec

• Input



• Output



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Analog Characteristics ($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data (Fs=44.1kHz)			0.0030	%
S/N ratio	S/N	1kHz, 0dB/– ∞ dB data (Fs=44.1kHz) (A filte used)	96			dB

Electrical Characteristics Testing Method

The testing of total harmonic distortion and S/N ratio is shown in Fig. 1. and 2.

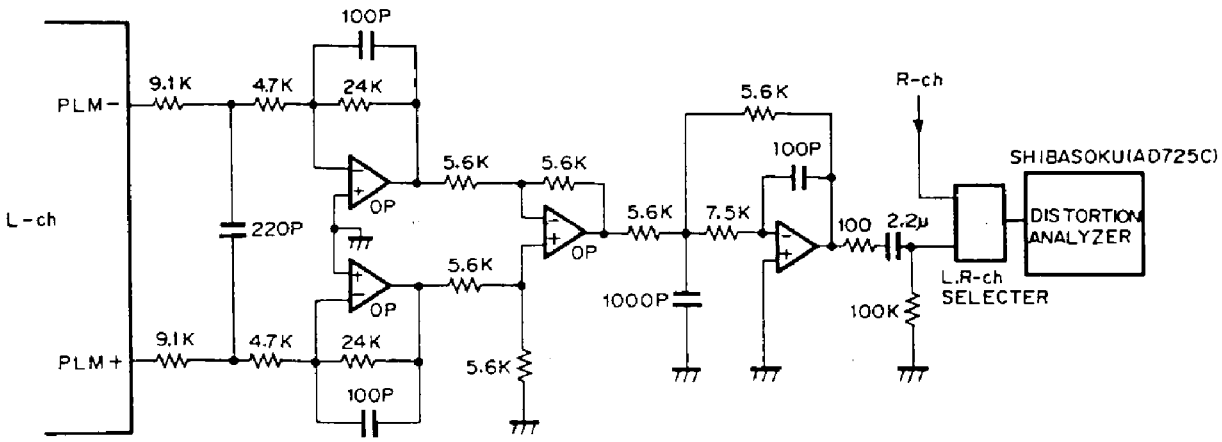


Fig. 1.

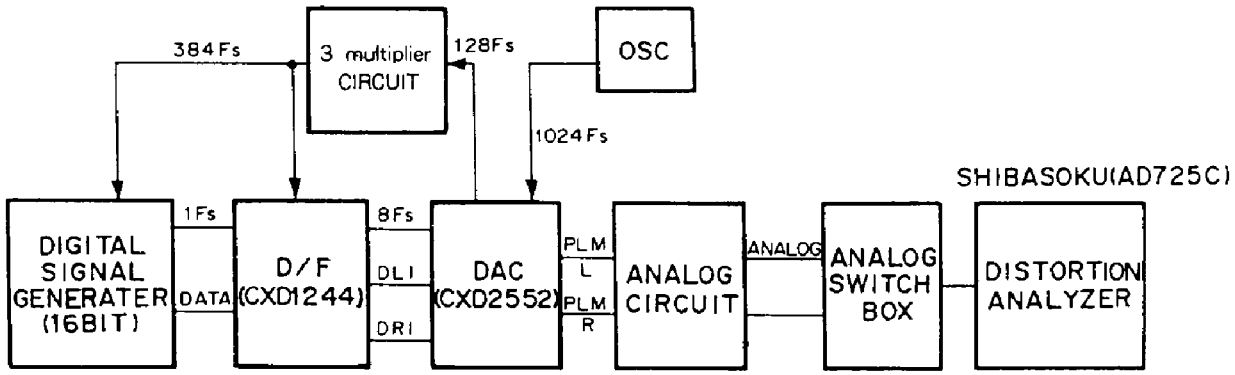


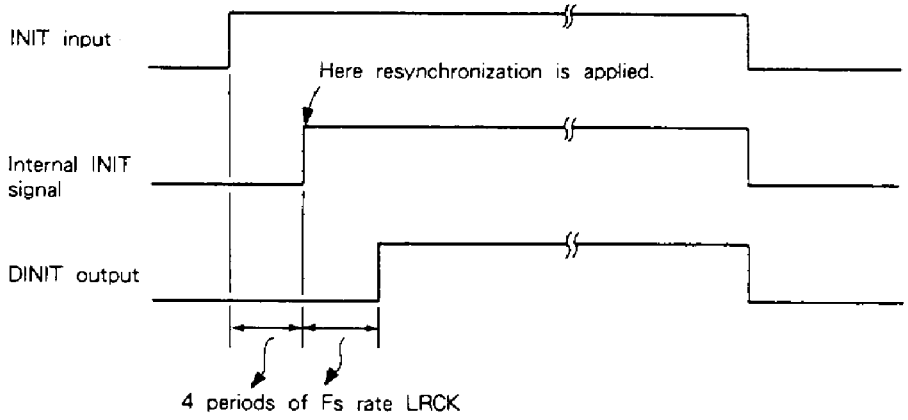
Fig. 2.

Description of Function

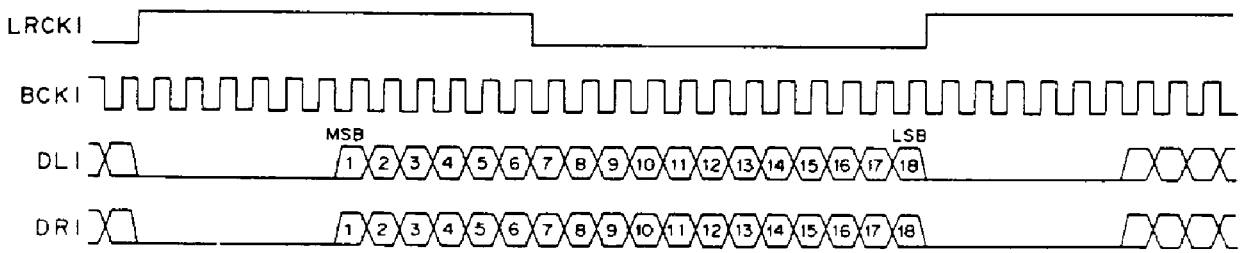
I/O Synchronizing Circuit

1) Theory of operation
A window featuring 8 internal clocks (256Fs) is set. The sync circuit observes whether the rising edge (LRCK ↓) of the LRCK input has entered the window or not.
When power supply is turned on, should LRCK ↓ be out of the window, the sync circuit stops the internal processing in timing with the center of the window. The processing is started synchronously with the appearance of the next LRCK ↓. Synchronization between the exterior system and this LSI is established through this operation.

2) Resynchronization by means of INIT
Even when LRCK ↓ is inside the window but located close to one of the two edges of the window, synchronization may be upset by the mingling of external noise. To this effect, it is necessary to apply resync without fail after power supply is turned on. Resync operation is executed from the rising edge of INIT and timed after 4 periods of Fs rate LRCK. The sync circuit is initialized and LRCK ↓ is located at the center of the window.
Moreover, when synchronization falls out of the window, INAF output turns to "H" level.



Input Timing (8fs rate)



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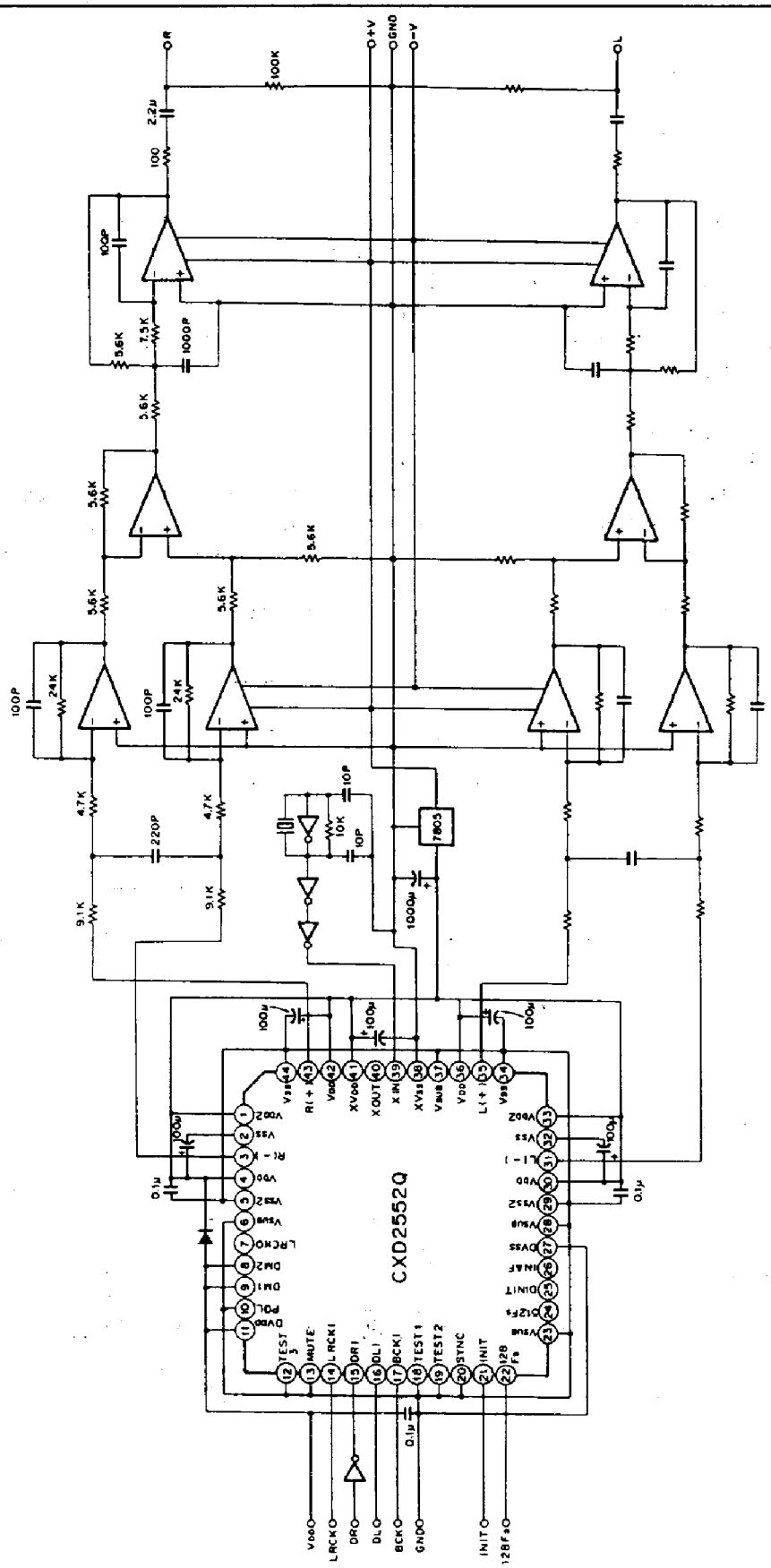
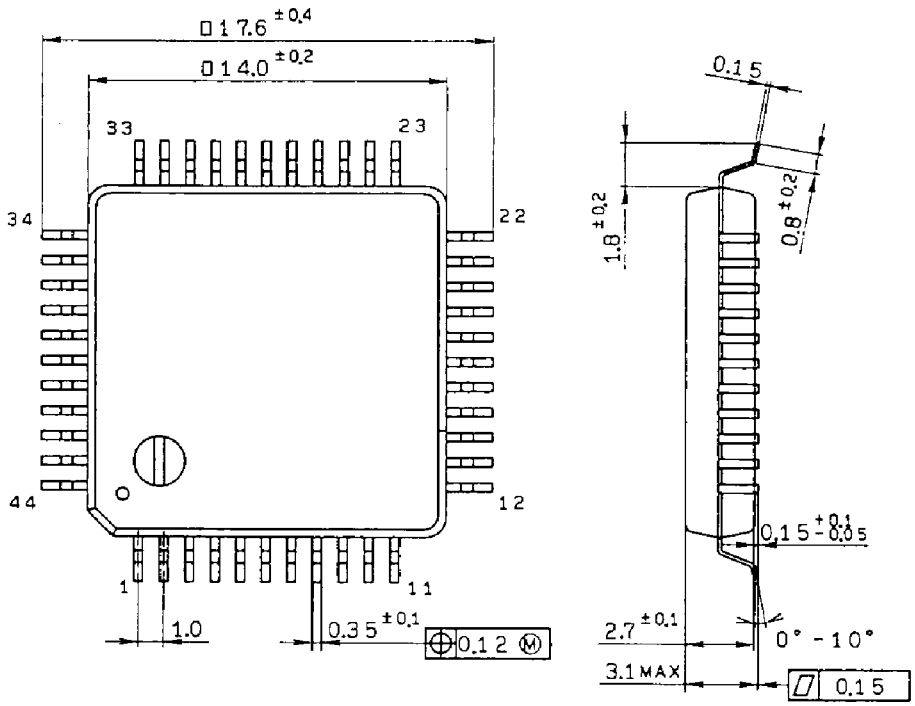
Application Circuit



Package Outline Unit : mm

44pin QFP (Plastic) 1.1g



SONY NAME	QFP-44P-L122
EIAJ NAME	*QFP044-P-1414-AX
JEDEC CODE	———

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Audio Delta Sigma Type A/D+D/A+D/F

ADVANCED INFORMATION

CXD2555Q is a delta sigma type (2nd order delta sigma noise shaping) A/D & D/A with a digital filter.

48pin QFP (Plastic)

Features

- Two Channel A/D, D/A with over-sampling, Decimation digital filter.
- Analog circuit for A/D included
- Distortion level: 0.01% (A/D, D/A)
- S/N: 90dB for D/A
  80dB for A/D

Functions

- 1 Fs data rate I/O possible
- Multi chip system possible
- Serial data inter face:32 slot
  Right/Left Adjusted Data
  MSB/LSB first in selections
- Master clock Selection:
  256Fs/512Fs/768Fs/1024Fs
- Fs selection:
  8KHz/16KHz/32KHz/44.1KHz/48KHz
- Provides several clock outputs, devided by a masterclock

Description of Operation

1. Serial Data Interface LRCK, BCK, SOUT, SIN, MASL, MLSL

Serial data format is same for both SIN and SOUT - 2's complementary 2 channel serial data. Each channel has 16bit data at 32bit slot. MASL mode select the 16bit data timing - data comes first or later. MLSL mode select MSB first or LSB first.

MASL	
H	Data First
L	Data Late

MASL	
H	MSB first
L	LSB first

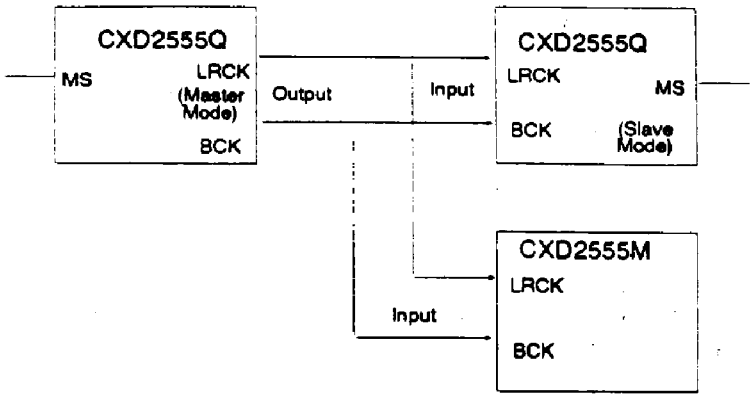
2. Master Mode/Slave Mode MS, LRCK, BCK

When multiple chips are used together, one of the ICs is used as "Master" and output LRCK, BCK. Other ICs are receiveing these clocks as "Slave" chips.

MS	Mode	LRCK, BCK I/O
H	Master Mode	Output
L	Slave Mode	Input

2. (Con't) Slave Mode

(Example)



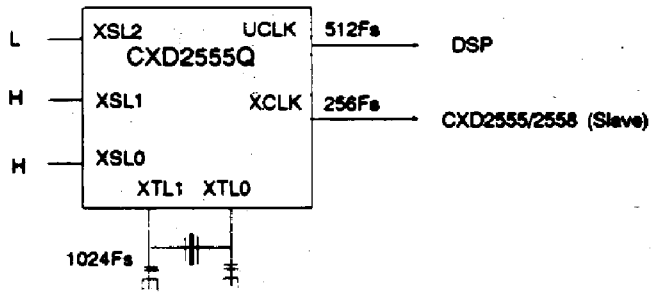
3. Crystal Oscillation Frequency Select XTLI, XTLO, XSLO, XSL1, UCLK, XCLK.

If XSL2 = "L" the crystal frequency is selected by XSL0 and XSL1 as shown in Table 1.
If XTLI receives CMOS level input signal, XTL0 should open.

XSL2	XSL1	XSL0	Crystal Freq	XCLK	UCLK
L	L	L	256Fs	256Fs	128Fs
L	L	H	512Fs	256Fs	256Fs
L	H	L	768Fs	256Fs	384Fs
L	H	H	1024Fs	256Fs	512Fs

Table 1 - Crystal Frequency Select

(Example)



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4. Low Frequency Fs Mode XTLI, XTL0, XSL0, XSL1, XSL2

If XSL2 = "H", Low frequency sample rate (Fs=8KHz, 16KHz) can be selected as shown in Table 2.

XSL2	XSL1	XSL0	Crystal Freq.	*Low Freq. Fs Mode
H	L	L	256x32KHz	16KHz
H	L	H	256x32KHz	8KHz
H	H	L	512x32KHz	16KHz
H	H	H	512x32KHz	8KHz

Table 2 - Low Fequency Fs Mode Select.

*32KHz based crystal frequency gives these Fs frequencies.
If 44.1KHz is base frequency then Low Frequency Fs are either 22.05KHz or 11.025KHz.
If 48KHz is base frequency then Low Frequency Fs are either 24KHz or 12KHz.

5. D/A Output Mode Selection

D/A Output Mode	Common	Differential
DASL0	L	H
DASL1	L	L

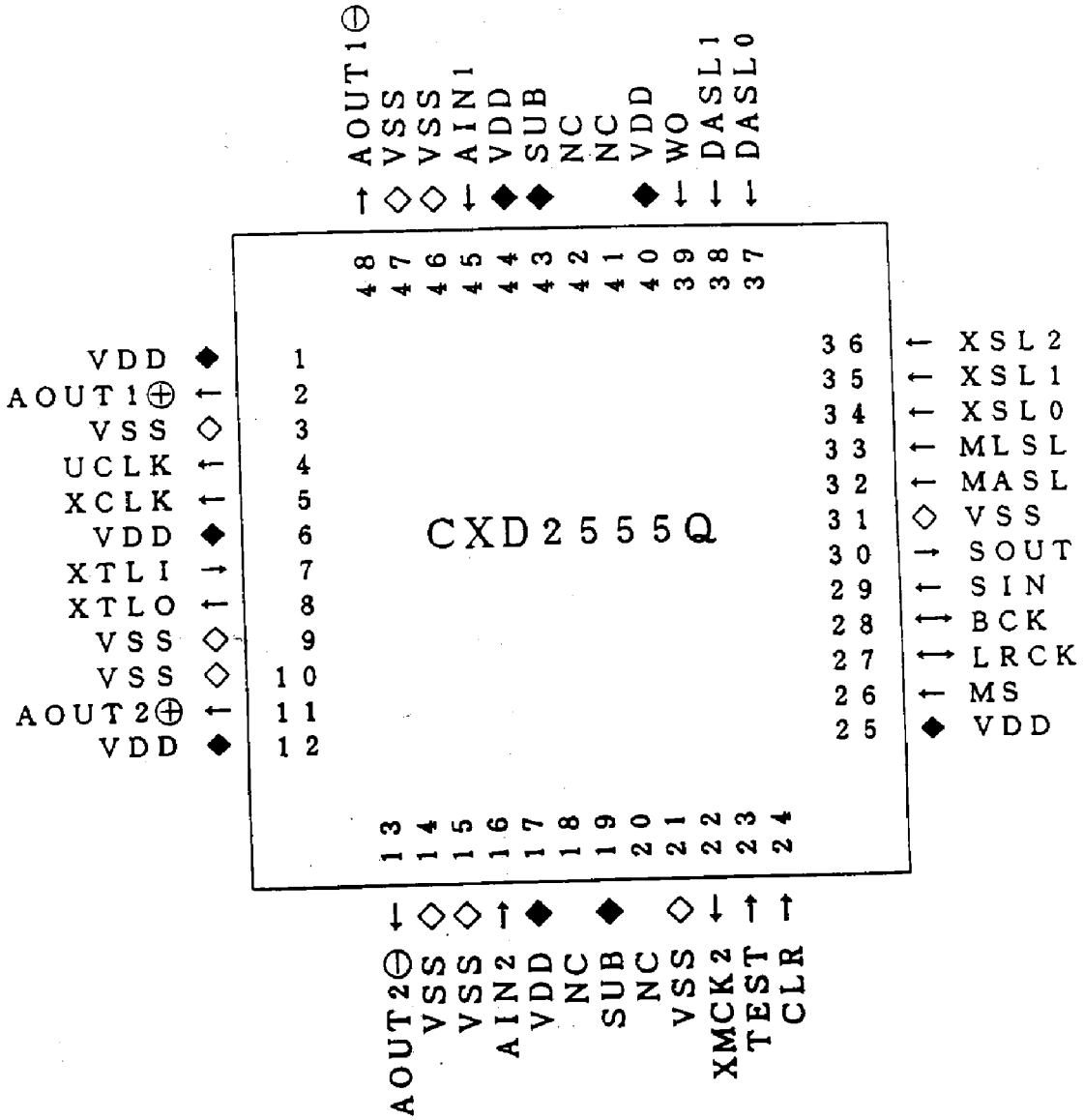
Mode Application
Common: Low output impedance, use "+" pin only.
Differential: Common noise cancel.

Pin Description

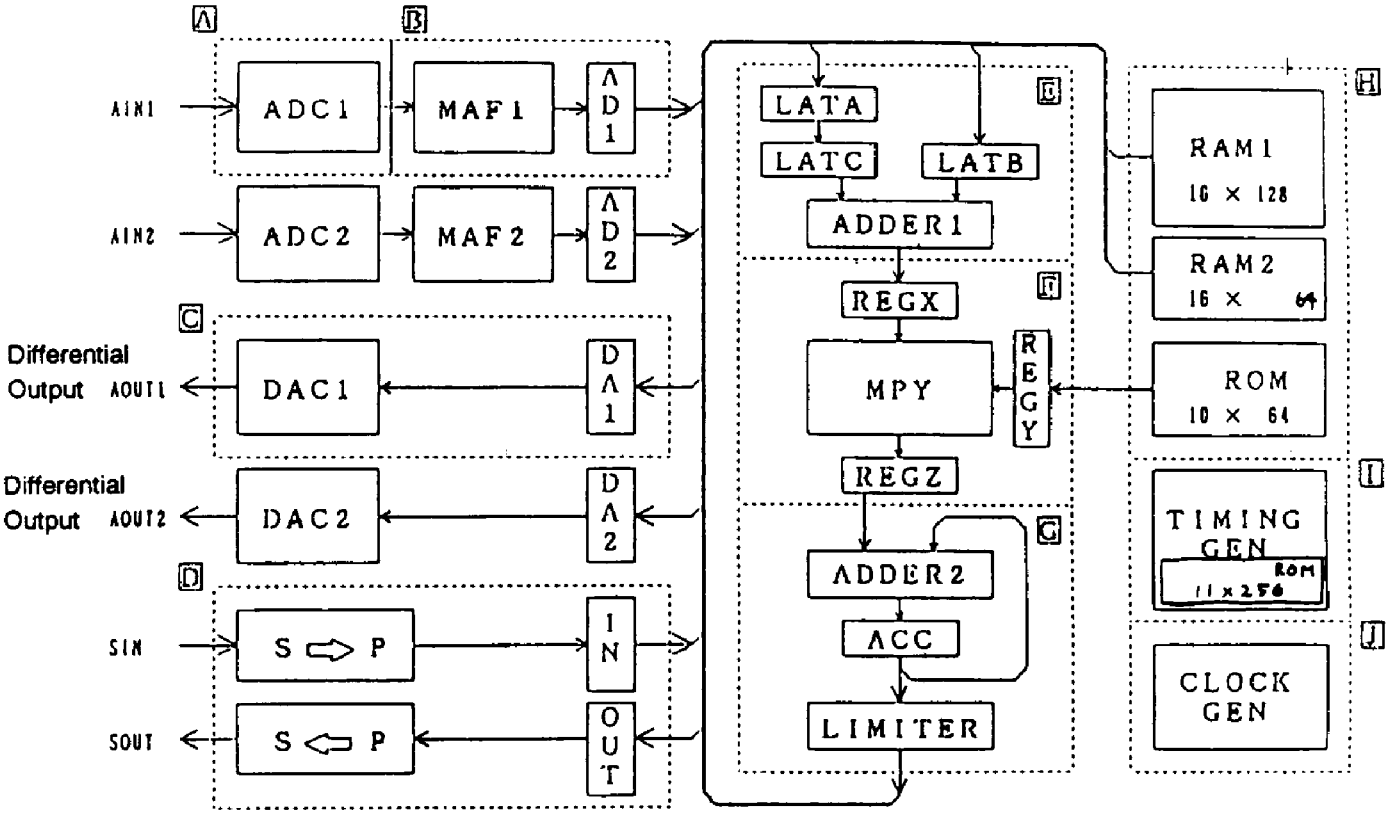
Pin No.	Symbol	I/O	Description
1	VDD	-	CH-1 D/A Analog Vcc
2	AOUT1+	O	CH-1 D/A Analog Output (+)
3	VSS	-	CH-1 D/A Analog GND
4	UCLK	O	User clock output 1/2 of master clock frequency
5	XCLK	O	256Fs Clock output
6	VDD	-	Digital Vcc
7	XTLI	I	Oscillating input for Master Clock. Crystal freq. is dependent upon the selection of XSLO 0~2
8	XTLO	O	Oscillating output for Master Clock
9	VSS	-	Digital GND
10	VSS	-	CH-2 D/A Analog GND
11	AOUT2+	O	CH-2 D/A Analog Output (+)
12	VDD	-	CH-2 D/A Analog Vcc
13	AOUT2-	O	CH-2 D/A Analog Output (-)

Pin Description (Con't)

Pin No.	Symbol	I/O	Description
14	VSS	-	CH-2 D/A Analog GND
15	VSS	-	CH-2 A/D Analog GND
16	AIN2	I	CH-2 A/D Analog Input
17	VDD	-	CH-2 A/D Analog Vcc
18	NC	-	
19	SUB	-	IC SUB terminal AC couple to GND
20	NC	-	
21	VSS	-	Digital GND
22	XMCK2	O	Over Sampling Clock Output (128Fs)
23	TEST	I	Test Pin
24	$\overline{CLR}$	I	$\overline{Clear}$ (Active Low)
25	VDD	-	Digital Vcc
26	MS	I	Master/Slave Selection "H"-Master Mode, "L"-Slave Mode
27	LRCK	I/O	If MS="H" Output Mode. If MS="L" Input Mode
28	BCK	I/O	If MS="H" Output Mode. If MS="L" Input Mode
29	SIN	I	Serial Data Input (2's complementary, 32bit slot)
30	SOUT	O	Serial Data Output (2's complementary, 32bit slot)
31	VSS	-	Digital GND
32	MASL	I	16bit serial data slot selection "H"-data first "L"-data late
33	MLSL	I	Selection for MSB first or LSB first "H"-MSB first "L"-LSB first
34	XSLO	I	Crystal Frequency Selection
35	XSL1	I	Crystal Frequency Selection
36	XSL2	I	Crystal Frequency Selection
37	DASL0	I	D/A Output Select
38	DASL1	I	D/A Output Select
39	WO	I	Window Open Mode "H"-Window Mask, "L"-Window Open
40	VDD	-	Digital Vcc
41	NC	-	
42	NC	-	
43	SUB	-	IC Subterminal AC Couple to GND
44	VDD	-	CH-1 A/D Analog Vcc
45	AIN1	I	CH-1 A/D Analog Input
46	VSS	-	CH-1 A/D Analog GND
47	VSS	-	CH-1 D/A Analog GND
48	AOUT1-	O	CH-1 D/A Analog Output (-)



ADC/DAC Block Diagram



Block Name

A : ADC
B : MAF
C : DAC
D : I/F
E : ADD
F : MPY
G : ACC
H : MEM
I : TIM
J : CLK

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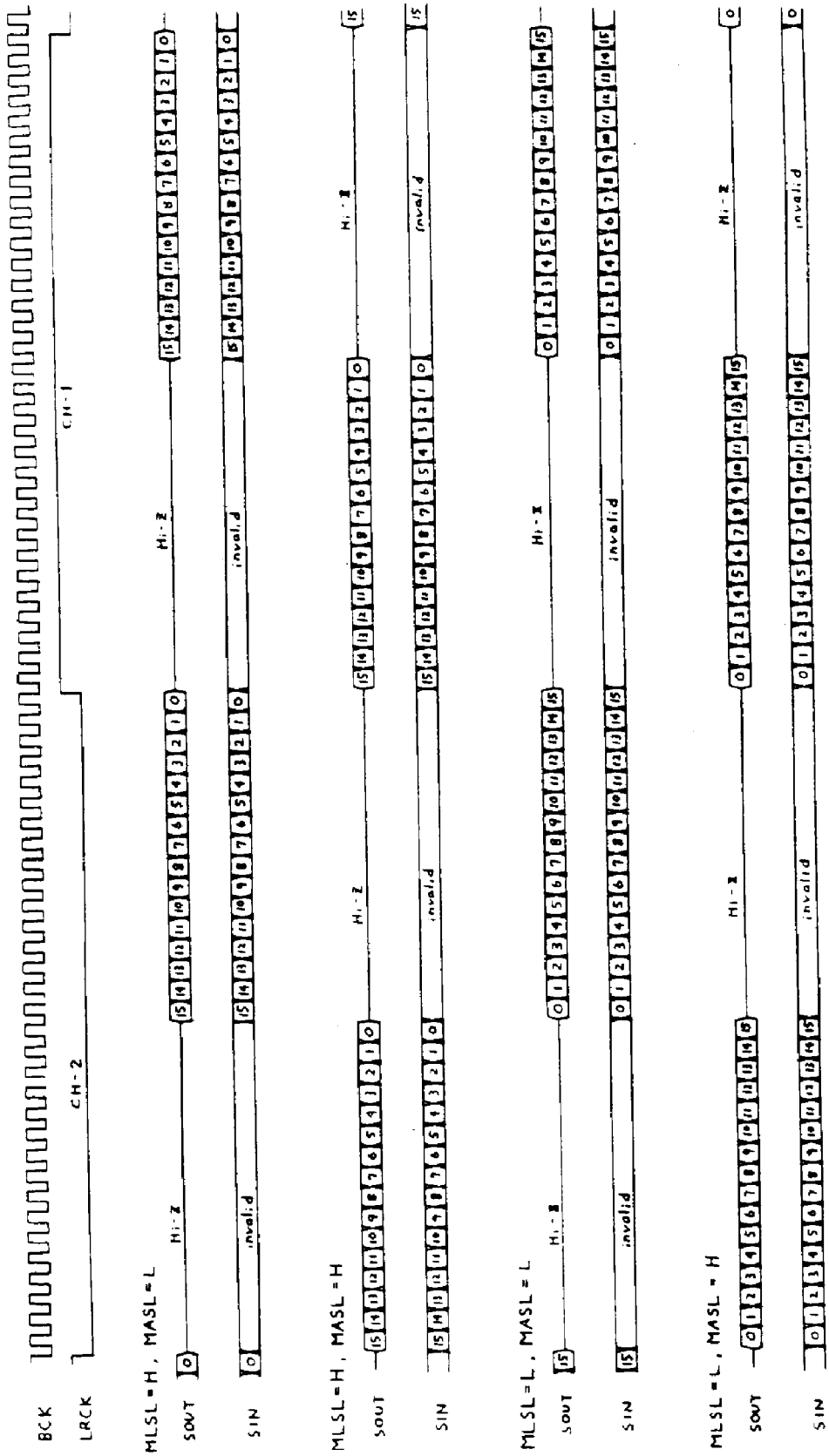

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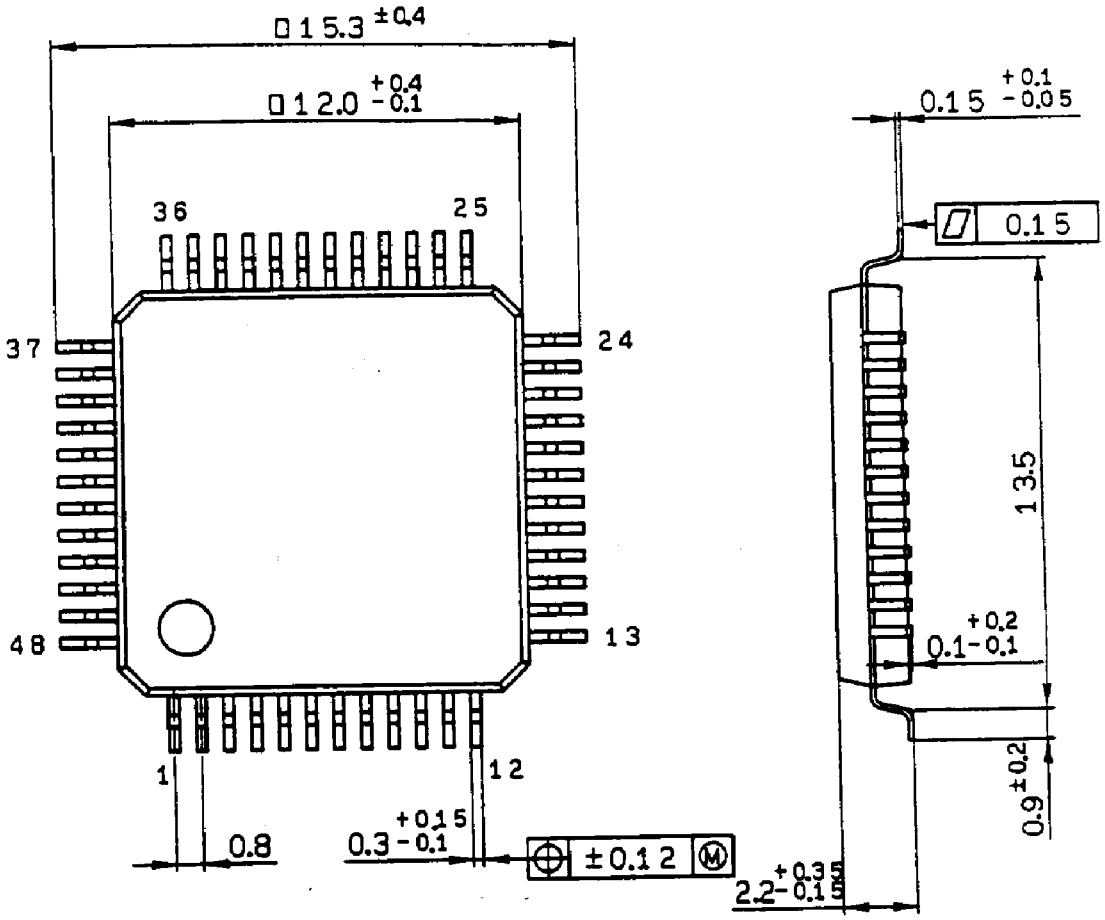

SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-8
JEDEC CODE	

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Test System